A 32-channel charge sensitive amplifier for delay-line readout of parallel plate avalanche counter array*

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Charge sensitive amplifiers for fast timing in delay-line readout of parallel plate avalanche counter (PPAC) array are designed. In total, 32 channels are realized on a single printed circuit board with operational amplifiers and other discrete components. Each channel is composed of an integrator, a pole-zero cancelation net, and a linear amplification stage, which can be accommodated to either positive or negative input signals. The design procedure is described in detail. The amplifier performance is calibrated with a signal generator. The gain approximately reaches ± 3 mV/fC with an RMS noise level of around 6 mV. In the application to a prototype PPAC, the amplifiers exhibit good practicality and stability.

Keywords: Charge sensitive amplifier, Fast timing, Discrete components, Delay line, Parallel plate avalanche counter

I. INTRODUCTION

Radiation detectors are widely used in heavy ion collision experiments to study nuclear structures and reactions. Kinematics of secondary protons, neutrons, or ions can be captured by the detectors. The coincident measurement of secondary particles and the particle-photon coincidence provide insights into the collision dynamics, energy level structure, or other internal states of the participants. Low pressure parallel plate avalanche counters (PPAC) [1, 2], semiconductor silicon detectors [3], and solid scintillation detectors [4, 5] are among the most commonly used detectors in the above-mentioned situations. Compared to scintillation detector, PPAC is especially suitable for fast timing and positioning applications. Sub-nanosecond and sub-millimeter resolution can be achieved simultaneously on a sensitive area of several hundred of cm^2. In comparison with silicon detectors, PPAC detectors are more radiation tolerant and cost efficient.

In order to study the Coulomb excitation of atomic nuclei [6], we are developing a PPAC array. It consists of 20 PPAC units, which could cover almost 4π solid angle around a solid target, similar to the CHICO2 array [1]. During the collision of the projectile and target nuclei, both of them could be excited by Coulomb interactions. Soon after their excitations, gamma rays are emitted during their deexcitations. The PPAC array detects the two-dimensional positions and the flight time difference of the recoil and scattered nuclei, so that nucleus identification and Doppler correction of the gamma-ray energy can be made [7]. Each PPAC unit is capable of sub-nanosecond timing precision, which is realized via the signal from the membrane electrode, and sub-millimeter position resolution, which is realized via the four signals from two perpendicular delay lines. The delay-line signals and the membrane signals have opposite polarities. They are immediately processed by the preamplifiers, which output negative voltage pulses to the following discriminators, i.e., both positive and negative detector current pulses should be converted to negative voltage pulses. Since each PPAC unit needs 5 readout channels, 100 channels are required in total.

The performance of the preamplifier contributes directly to the resolution of the detector system. Various customized preamplifiers have been developed to adapt to different detectors. The integration scheme of multichannel preamplifiers can be roughly classified into three ways. First, integration in detector of semiconductor pixel application specific integrated circuits (pixel ASIC), such as the TaichuPix [8], JadePix [9], Timepix [10], Supix [11], ALPIDE [12], Topmetal [13], Nupix [14], IMPix [15], etc. The preamplifier, together with certain following electronic stages, is photoetched adjacent to the detector sensor in the same bulk, or connected to the sensor via eutectic solder bumps. The pixel size is several tens to hundreds of micrometers, which offers micrometer position resolution. These pixel ASICs find applications as the vertex or tracking detectors in large-scale collider experiments, where thousands or more high-density electronics are required [8–12], or in places of ultra-high position resolution, such as beam telescopes [16], X-ray imaging [17], etc. Second, chip level integration. Encapsulation of several to more than a hundred channels of font-end electronics (FEE), including the preamplifier stage, has been realized in one semiconductor chip. Typical examples are

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the SAMPA [18], PIST [19], AGET [20], the ASIC developed for CdZnTe and Si-PIN detectors in [21], and the micromegas readout ASIC in [22], to name a few. The Connection between the detector readout electrodes and the FEE is established via transmission lines, usually on a printed circuit board (PCB). Separation of the FEE from the detector releases the limitation on the detector patch size, as encountered in pixel ASICs, while still retains high circuit density. Hence, this scheme is widely adopted in large-area detectors and other situations where high density readout electronics are pursued, e.g., the time projection chamber (TPC) in the ALICE experiment [18], micro-pattern gaseous detectors [22, 23], avalanche-photodiode array detectors [24], the silicon tracker and BGO calorimeter on the DAMPE satellite [25, 26], the Compton telescope for dose monitoring in hadron therapy [27], the detectors in positron emission tomography (PET) [28, 29], etc. Third, board level integration. Typically, several to tens of channels can be realized on one PCB. Each channel is constructed with discrete elements, including operational amplifiers (OPA), resistors, capacitors, etc. This solution is usually adopted in situations where several to hundreds of channels are required and where board level circuit density is acceptable. Compared to the chip level realization, the dynamic range and circuit logic can be adjusted more conveniently and economically to meet various requirements, by selecting adequate elements from the vast commercial market. Typical applications can be found in the SPA02-16 and SPA03-16 preamplifier modules for silicon detectors [30], the multi-purpose TPC at CSNS Back-n [31], the NEXT experiment in search of $0\nu\beta\beta$ decay [32, 33], the scintillation detector array designed for PET [34, 35], the CZT-based gamma-ray spectrometer [36], and the ITER radial X-ray camera [37], etc.

In this work, the third scheme is adopted. A versatile 32-channel charge sensitive amplifier (CSA) is designed for the PPAC array under development. In what follows, Section II describes the schematic and PCB design of the amplifier, Section III presents the performance calibrations with a signal generator and an oscilloscope, Section IV shows the test results in the application to a prototype PPAC, and Section V concludes this work.

II. SCHEMATIC CIRCUIT DIAGRAM AND PCB DESIGN

Typical PPACs use the delay-line readout scheme [38], which requires fast timing amplifiers. The characteristic fast response of PPACs is listed in table 1. Totally 10^6 to 10^7 electron-ion pairs could be generated in an avalanche multiplication [39, 40]. However, only $\sim 10\%$ of the total electrons contribute to the fast signal [38, 41]. The rise time is normally 5-10 ns [38–42]. The full width is around 15 ns [39, 41]. Accordingly, the maximum current is estimated to be several micro-amperes.

The preamplifier is designed to convert the PPAC output charge to a voltage pulse of several hundred mV in amplitude. The width of the voltage pulse is set to the same order as the original detector response time, so that high counting rates can be realized.

TABLE 1. Typical fast response of PPAC detectors.

Current Rise Time	Current Width	Current Maximum	Total Avalanche Electrons
6 ns [38] 8 ns [39] [1] 10 ns [41] 5 ns [42]	20 ns [39] [1] 15 ns [41]	several μA [2]	$10^6 \sim 10^7$ [39] [3] 10^6 [40] [3]

[1] Before the launch of space-charge effect.
[2] Estimation based on the shape and total charge in the fast current pulse induced by electrons.
[3] Only $\sim 10\%$ of all the electrons induce the fast pulse [38, 41], i.e., in the order of 10^5.

A. Schematic Design

Each CSA channel is composed of two stages of OPA circuit. The first stage is a charge integrator (Qint). The second is a noninverting amplification (NinvAmp) or inverting amplification (InvAmp) stage, designed for different detector response polarities. Fig. 1 shows the schematic diagrams, i.e., (a) Qint + NinvAmp and (b) Qint + InvAmp, respectively. The Qint input is AC coupled to the detector electrode via a single-ended transmission line of 50 Ω. In order to control the noise level in the Qint output, a long decay time constant of 1 μs is set. It leads to noteworthy signal pile-up and DC voltage shift at high counting rates. Therefore, a pole-zero cancelation (PZC) net is inserted between the Qint stage and the following linear amplification stage.

The OPA657 [43] and OPA847 [44] produced by the Texas Instruments Incorporated Company are adopted in the first and second amplifier stages, respectively. OPA657 and OPA847 are voltage feedback amplifiers. Both of them feature very low input voltage noise density, while the JFET-input stage endows OPA657 with much lower input current noise density and input bias current. Hence, using OPA657 in the first stage favors lower noise and higher DC precision at the output.

The signal to noise ratio (SNR) of the final output is principally determined by the SNR of the Qint output. As a balance between the noise level and conversion gain, the feedback capacitor $C_{f1}^{int} = 5$ pF and feedback resistor $R_{f1}^{int} = 200$ kΩ are chosen (the parasitic capacitance in parallel with C_{f1}^{int} is about 0.1 pF). The time constant $\tau_{int} = R_{f1}^{int} C_{f1}^{int} = 1$ μs. The gain of the Qint stage is $G_{int} = 1/C_{f1}^{int}$ in the normal operating condition of $A_{ol} C_{f1}^{int} \gg C_s + C_{f1}^{int}$, where C_s is the total input capacitance and A_{ol} is the OPA open loop gain. In order to stabilize the Qint circuit, the resistor $R_{g1}^{int} = 10\ \Omega$ in series with the capacitor $C_{g1}^{int} = 10$ pF is installed for input lag compensation. The coupling capacitor C_c is set to 10 nF, the self-resonant frequency of which is close to the input signal bandwidth. The resistor $R_c = 50\ \Omega$ is the termination resistor for terminal matching to the 50 Ω input transmission line.

The gain of the InvAmp stage $G_{inv} = -R_{f1}^{inv}/R_{g1}^{inv}$ and

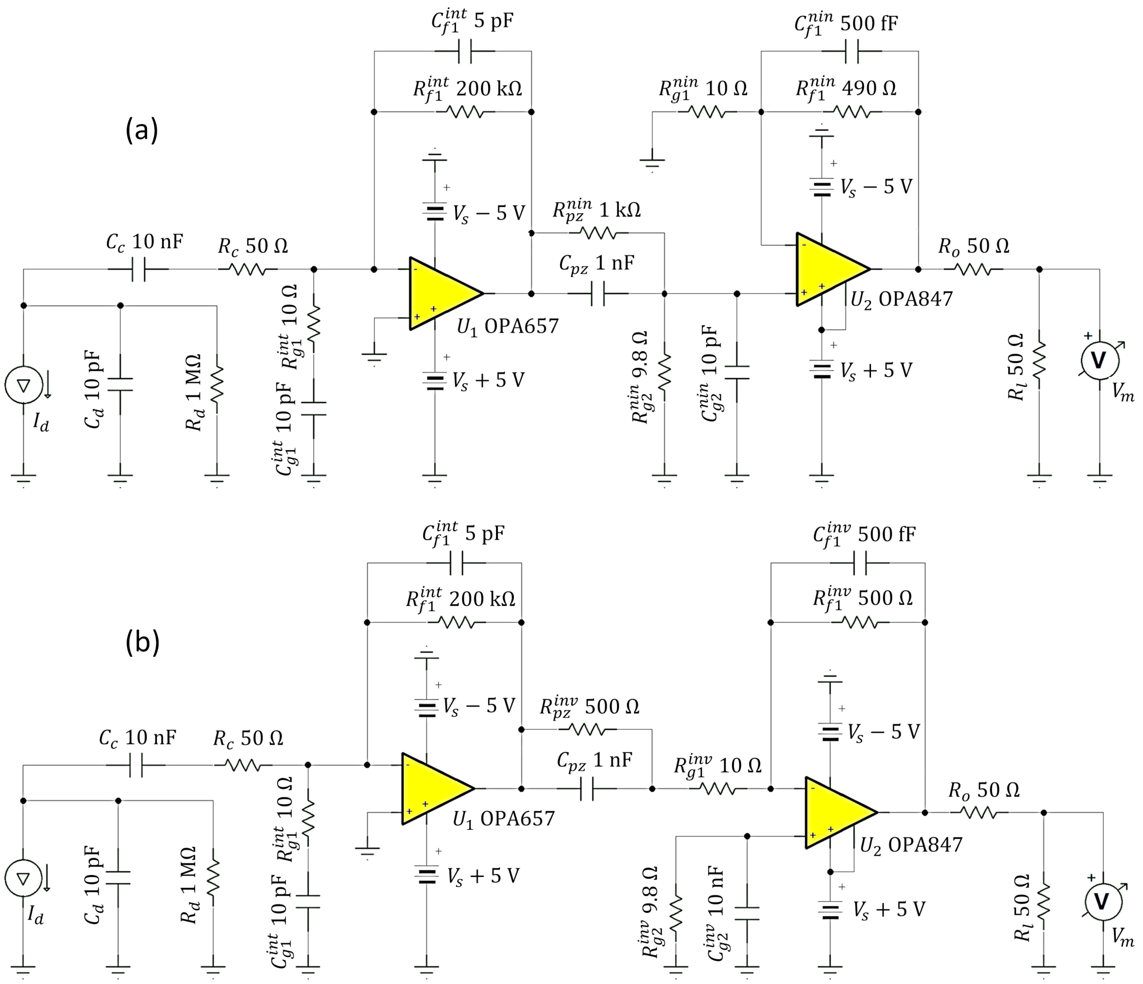

Fig. 1. Schematic diagrams of the CSAs. (a) Qint + NinvAmp. (b) Qint+ InvAmp. Note that a PZC net is inserted between the two OPA circuits in each CSA. The components before the capacitor C_c simulate the detector response. R_l is the load resistor.

the NinvAmp stage $G_{nin} = 1 + R_{f1}^{nin}/R_{g1}^{nin}$ are tuned by adjusting the four resistors. The feedback resistors are $R_{f1}^{inv} = R_{f1}^{nin} = 500\ \Omega$. The resistors R_{g1}^{inv} and R_{g1}^{nin} are fixed at $10\ \Omega$. The capacitors C_{f1}^{inv} and C_{f1}^{nin}, together with the parasitic capacitance in parallel with them, function as feedback lead compensation to stabilize the circuit operation. After fine adjustment, $C_{f1}^{inv} = C_{f1}^{nin} = 0.5$ pF are installed. The pull-down resistors $R_{g2}^{inv} = R_{f1}^{inv} \| R_{g1}^{inv} \approx 9.8\ \Omega$ and $R_{g2}^{nin} = R_{f1}^{nin} \| R_{g1}^{nin} \approx 9.8\ \Omega$ at the noninverting input of the OPA847 chips suppress the output DC error caused by the input bias current. The capacitors $C_{g2}^{inv} = 10$ nF and $C_{g2}^{nin} = 10$ pF are in parallel with R_{g2}^{inv} and R_{g2}^{nin}, respectively. These two capacitors minimize the output noise contribution from the resistors, without too much impact on the PZC net. The resistor $R_o = 50\ \Omega$ is for source-end impedance matching to the $50\ \Omega$ output transmission line.

The gain bandwidth product of OPA847 is $GBW_{847} = 3.9$ GHz. The critical input amplitude of OPA847 before the start of slew rate limitation is $V_{crit}^{847} = SR_{847}/2\pi GBW_{847} = 38.8$ mV, where $SR_{847} = 950$ V/μs is the slew rate. For 50 V/V gain, it corresponds to 1.9 V output voltage. The full power bandwidth (FPB) of OPA847 at ±5 V power supply is $FPB_{847} = SR_{847}/2\pi V_{sat}^{847} = 45.8$ MHZ, where $\pm V_{sat}^{847} = \pm 3.3$ V is the output voltage swing.

In the Qint + NinvAmp configuration, the PZC circuit is composed by $C_{pz}^{nin} = 1$ nF, $R_{pz}^{nin} = 1$ kΩ, and $R_{g2}^{nin} = 9.8\ \Omega$. Thus, the condition $\tau_{rc}^{nin} = R_{pz}^{nin} C_{pz}^{nin} = \tau_{int}$ is fulfilled. However, in the Qint + InvAmp configuration, the PZC circuit consists of $C_{pz} = 1$ nF, $R_{pz}^{inv} = 500\ \Omega$, and $R_{g1}^{inv} = 10\ \Omega$, which breaks the equality, $\tau_{rc}^{inv} = R_{pz}^{inv} C_{pz}^{inv} \neq \tau_{int}$. If R_{pz}^{inv} were set to 1 kΩ to force the equality, significant overshoot would appear at the end of the decay edge. This might be due to the fact that the inverse input of the OPA847 is not virtual ground anymore because of the existence of $R_{g2}^{inv} \| C_{g2}^{inv}$. Setting $R_{pz}^{inv} = 500\ \Omega$ in the present circuits, the overshoot and the resultant overcompensation are both at the noise level, as shown in Fig. 3. The decay time constant of the PZC output signal is $\tau_{pz} \approx 10$ ns.

For the input charge of 10^5 to 10^6 equivalent electrons, the Qint output pulse height is expected to be 3.2 mV to 32 mV. The PZC net roughly halves the amplitude to 1.6 mV to 16 mV due to ballistic deficit. This signal is further amplified by

51 times in the NinvAmp stage or -50 times in the InvAmp stage. At last, the impedance matching resistor R_o halves the voltage transmitted to the following 50 Ω transmission line. Therefore, the final output pulse height ranges from 40 mV to 400 mV. This corresponds to an estimated conversion gain of 2.5 mV/fC, which coincides with the calibrated gain in Section III B.

B. PCB Layout and Routing

On a rectangular $10\ \mathrm{cm} \times 20\ \mathrm{cm}$ PCB, 4×8 preamplifiers are realized in a planar array, as shown in Fig. 2. The pad layout and routing are the same in every unit. By setting some pads DNP (do not populate), a wide freedom is accessible in adjusting the circuits. Thus, both CSA circuits can be implemented. In Fig. 2, the 1st and 3rd rows are Qint + NinvAmp amplifiers, while the 2nd and 4th rows are Qint + InvAmp circuits. At the input and output, the signals are routed through a surface mounting board-to-board (BTB) connector. Adjacent signal pins on each connector are isolated by a pair of pins which are independently connected to the power plane and the ground plane, respectively. This pin configuration minimizes the connector-mediated crosstalk, unifies the signal return path, also contributes to reducing the power-ground impedance. The two LEMO connectors soldered on the bottom are for power supply in the circuit test phase.

TABLE 2. PCB stackup design. GND denotes the ground plane. PWR denotes the power plane.

Layer	Routing
1 (top)	component layer
2	GND
3	signal
4	PWR, +5 V
5	signal
6	GND
7	signal
8	PWR, -5 V
9	signal
10 (bottom)	GND with a few components

The stackup is composed of ten layers, which are listed in table 2. The second and bottom layers are both ground plane for better electromagnetic compatibility (EMC). Between them, four signal layers are interleaved with the ground or power planes. Thus, all the 32 input signal traces and 32 output signal traces are striplines, which are routed in parallel. The impedance of the signal traces is adjusted to 50 Ω with the trace width set to 9 mil. The smallest separation in the direction parallel to the PCB surface between two adjacent traces is at least 120 mil if they are in the same layer, 60 mil if they are in adjacent signal planes, and 0 if they are three layers apart. Except for 16 parallel signal traces (8 input, 8 output) on each signal plane, the rest area is poured with grounded copper, which provides even better decoupling for the power planes. A grounded guard ring is laid around each channel on the top layer to suppress crosstalk. Stitching vias are thoroughly used on the guard rings, along the PCB border, and along both sides of every signal trace.

III. PERFORMANCE TESTS

The Qint + NinvAmp and Qint + InvAmp channels used in the performance calibrations are indicated in Fig. 2 by (a) and (b), respectively. The amplitude-frequency characteristic and linearity are tested by connecting a resistor $R_{test} = 20\ \mathrm{k}\Omega$ in series with the capacitor C_c. A series of voltage signals are fed to each circuit through R_{test}. The resistor converts the voltage signals into current signals, while the input charge signals are simply the integration of the respective current signals. The amplitudes of the output signals are measured with an oscilloscope (12 bit analog-to-digital converter, 1.5 GHz bandwidth, 2.5 GS/s sampling rate). Fig. 3 presents the output of the CSAs, together with the equivalent input charge signal. The rising time, falling time, and full width at half maximum of the input voltage pulse are 2 ns, 2 ns, and 10 ns, respectively. The leading edges of the input charge signal, the Qint + NinvAmp output, and the Qint + InvAmp output signals are 8.1 ns, 7.1 ns, and 7.4 ns, respectively. The amplitudes are -481.5 fC, 1.326 V, and -1.471 V, respectively.

A. Bandwidth

Sinusoidal voltage signals of frequencies 1 MHz to 100 MHz are fed to each circuit via the R_{test} resistor. The amplitudes of the output signals are measured with an oscilloscope. The amplitude-frequency responses are drawn in Fig. 4. The -3dB bandwidths of the Qint + NinvAmp and Qint + InvAmp circuits are determined as 18 MHz and 21 MHz, respectively. As analyzed in Section II A, the bandwidth of the linear amplification stage is much larger than the measured bandwidths. Hence, they are dominated by the Qint stage and the PZC net, which coincides with the decay time constant of $\sim$ 10 ns. The leading edge of the PZC output is typically faster than the decay edge considering that the full width of the PPAC response is smaller than 20 ns, which is also exemplified in Fig. 3.

B. Linearity

The input charge signals are similar to that shown in Fig. 3, only differing in the total input charge. The evolution of the output pulse amplitude with the total input charge is shown in Fig. 5. The conversion gain is determined by fitting the corresponding data, which are -2.772 mV/fC and 3.083 mV/fC for the Qint + NinvAmp and Qint + InvAmp circuits, respectively. The measured input ranges are -14.4 fC to -577.8 fC and -14.4 fC to -529.7 fC, respectively. The corresponding linear correlation coefficients are -0.99989 and 0.99990. The corresponding integral nonlinearities are $\pm 1.46\%$ and $\pm 1.29\%$. The energy deposition of an incident particle inside a PPAC and the charge avalanche amplification exhibit

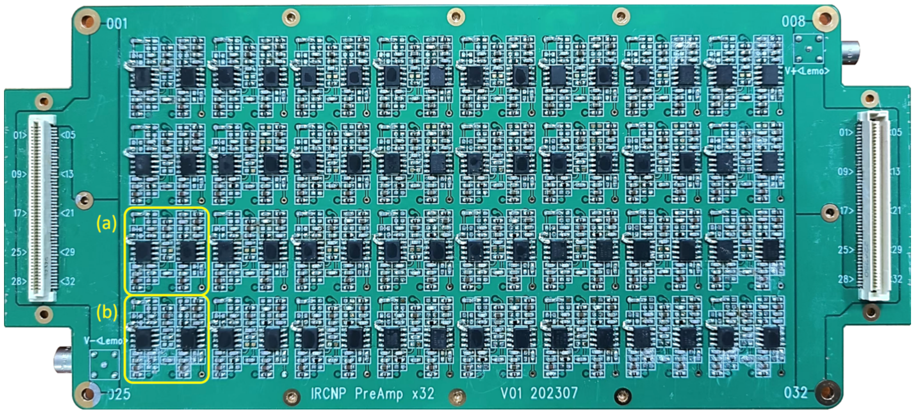

Fig. 2. Photograph of the PCB. The 1st and 3rd rows are Qint + NinvAmp amplifiers. The 2nd and 4th rows are Qint + InvAmp circuits. (a) and (b) indicate the Qint + NinvAmp and Qint + InvAmp channels used in the following performance tests, respectively.

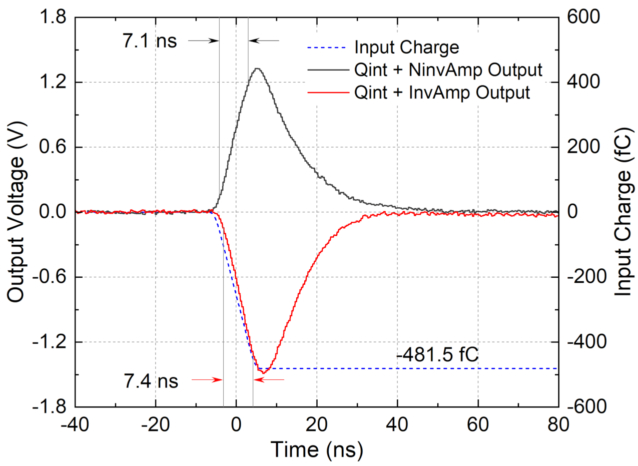

Fig. 3. A sample of an input charge signal (dash) and the corresponding output voltage signals by the Qint + NinvAmp (positive pulse in solid line) and Qint + InvAmp (negative pulse in solid line) amplifiers.

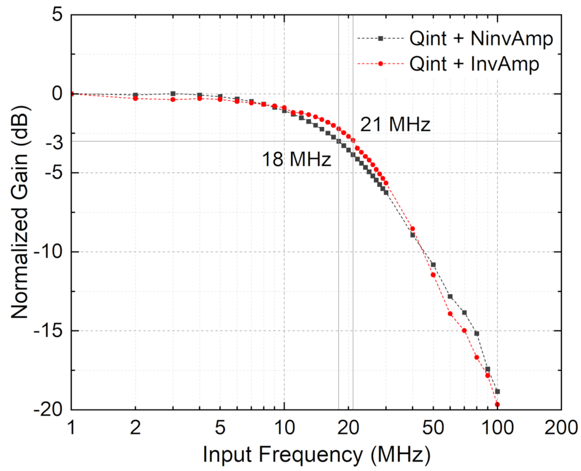

Fig. 4. Amplitude-frequency response curves of the two circuits. Frequencies wrote by the side of the vertical reference lines indicate corresponding -3dB bandwidths.

considerable fluctuations, much larger than the measured integral nonlinearities. Hence, the present circuit linearities are acceptable.

C. Noise and Baseline

The evolution of the RMS noise with the detector capacitance is measured. The detector capacitance C_d is mimicked by a capacitor soldered between the channel input pad and a ground pad under the input BTB connector. The data are shown in Fig. 6. Each data set is fitted with a cubic polynomial. Corresponding to the Qint + NinvAmp and Qint + InvAmp circuits, the zero-capacitance RMS noises are 5.85 mV and 6.59 mV, respectively. The noise evolution is dominated by the linear coefficients, which are 6.58×10^{-2} and 9.27×10^{-2}, respectively. The noise evolution is further modified by the quadratic coefficients, -5.01×10^{-4} and

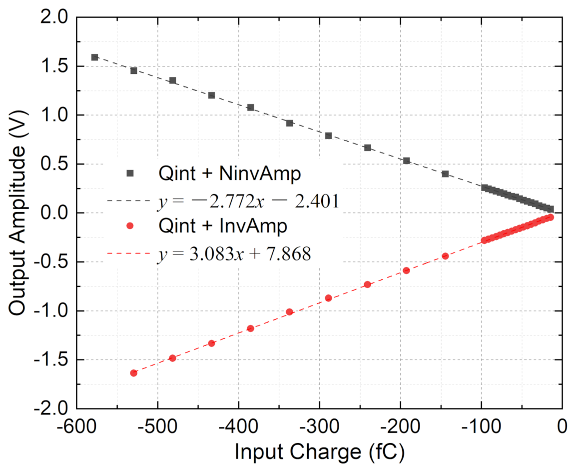

Fig. 5. Variation of the output pulse amplitude with the total input charge for the Qint + NinvAmp and Qint + InvAmp circuits.

-9.84×10^{-4}, and the cubic coefficients, 1.60×10^{-6} and 4.37×10^{-6}, respectively. The maximum base line shift of each output in varying the detector capacitance is 1.35 mV and 6.12 mV, respectively, both of which are smaller than the corresponding RMS noise.

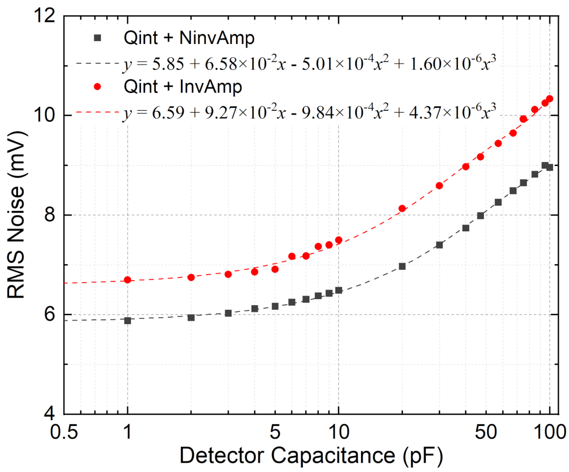

Fig. 6. Evolution of the CSA output RMS noise with the detector capacitance. The detector capacitance is mimicked by a capacitor soldered on the back side of the input BTB connector.

D. Crosstalk

Crosstalk between channels is measured as follows. A charge signal identical to that in Fig. 3 was fed to one channel. A 50 Ω resistor load was installed at the output of this channel on the back side of the output BTB connecter. Then, the output of any other channels was observed with the oscilloscope via the corresponding pins of the BTB connecter. It turns out that the waveforms didn't show any difference whether the input charge signal existed or not. Hence, it can be concluded that the crosstalk between any channels is completely submerged by the noise.

IV. APPLICATION IN PPAC

The practicality of the CSAs is verified with a home-made PPAC. It is a prototype of one unit of the aforementioned PPAC array under development, which is used for proof of principle. It mainly consists of a cathode membrane and an anode readout PCB, as sketched in Fig. 7, the details of which will be described elsewhere. The Cartesian coordinates (x, y) of an incident particle can be readout independently with two delay lines on the anode. During the test, an aperture mask is installed on the top of the membrane, which is also shown in Fig. 7. Alpha particles of ~ 5.4 MeV energy passing through the apertures are detected.

Typical waveforms from the CSAs are shown in Fig. 8. The trigger signal (S_0) is readout from the membrane by one Qint + NinvAmp amplifier. The other four signals

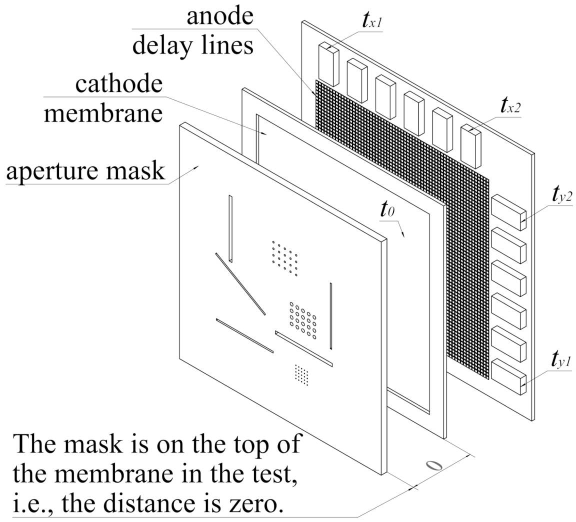

Fig. 7. Sketch of the PPAC used in the test. The index arrows beside t_0, t_{x1}, t_{x2}, t_{y1}, and t_{y2} indicate the positions from which the corresponding time signals are readout.

$(S_{x1}, S_{x2}, S_{y1}, S_{y2})$ are readout from the two delay lines by four Qint + InvAmp amplifiers. Note that, the membrane signal and the rest delay-line signals are from two independent events with no temporal correlation. They are drawn together merely to illustrate the common temporal sequence, i.e., the membrane signal comes earlier than the delay-line signals. The leading small positive peak and the following large negative peak in each delay-line signal indicate that the output current pulses from the delay lines are bipolar, which might be caused by the induction between the membrane and the anode.

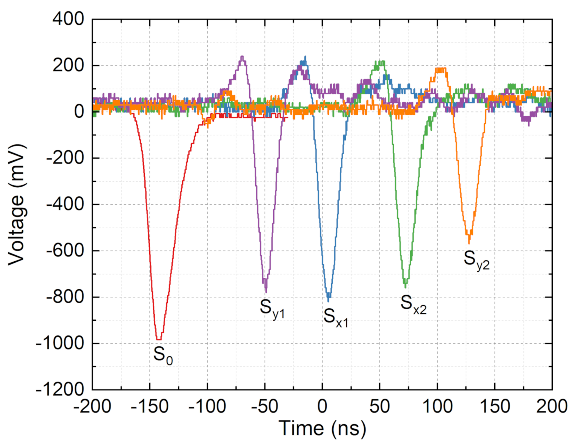

Fig. 8. Waveforms from one Qint + NinvAmp amplifier (S_0) and four Qint + InvAmp amplifiers $(S_{x1}, S_{x2}, S_{y1}, S_{y2})$. S_0 is the signal from the membrane in an event. S_{x1} and S_{x2} $(S_{y1}$ and $S_{y2})$ are the signals from the delay line in the $x(y)$ direction in another event.

The five analog signals from the CSAs are fed to a constant fraction discriminator, ORTEC CF8000 [45]. The five logic signals from the discriminator are further processed by the CAEN time-to-digital converter (TDC) module V775 [46].

The digital times of the four delay-line signals, t_{x1}, t_{x2}, t_{y1}, and t_{y2} are measured relative to the trigger time t_0, the later of which signifies the particle arrival time. The coordinates are calculated by $x = \frac{t_{x1}-t_{x2}}{t_{x1}+t_{x2}-t_s} \times HL$ and $y = \frac{t_{y1}-t_{y2}}{t_{y1}+t_{y2}-t_s} \times HL$, where $HL = 30$ mm is the half length of the detector in either the x or y direction and $t_s = 3318$ is fitted from the measured mask pattern. As shown in Fig. 9, the measured pattern faithfully matches the aperture mask geometry.

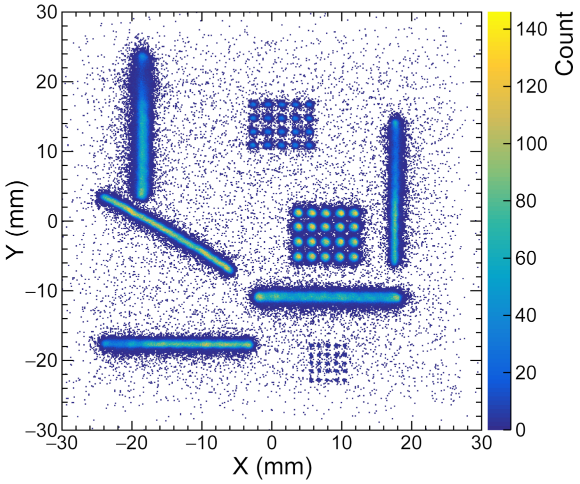

Fig. 9. Aperture pattern measured in the test.

V. SUMMARY

In summary, a 32-channel preamplifier is designed for a PPAC array under development for Coulomb excitation studies of atomic nuclei. It is realized on a 10 cm × 20 cm PCB with OPAs and other discrete components. Each channel is charge sensitive, essentially consisting of an integrator, a pole-zero cancelation net, and a linear amplification stage. Each channel can be configured to accommodate either positive or negative input, which is named Qint + NinvAmp and Qint + InvAmp, respectively. Corresponding to the two circuits, the bandwidths are 18 MHz and 21 MHz, the integral nonlinearities are $\pm 1.46\%$ and $\pm 1.29\%$, the zero-capacitance noises are 5.85 mV and 6.59 mV, respectively. The baseline shift of either circuit is smaller than the RMS noise. No crosstalk between any channels is observable, thanks to the PCB layout and routing design. In the application to a prototype PPAC, both circuits exhibit good practicality and stability. Hence, this multichannel preamplifier is expected to be used in the PPAC array in the future.

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Data availability: The related data are available from the corresponding author under reasonable request.

Declarations of Conflict of Interest: The authors declare no competing interest.

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